REMARKS

Claims 1, 12, 14, 19-21, 29 and 30 have been amended as indicated above. Claim 31 has been canceled. No new matter has been added.

I. Claim Objections

Claims 14 and 31 are objected to on the grounds that they are "formulated unclear in terms of what 'fails.'" Claim 14 has been amended to more clearly identify the item to be tested for failure. Claim 31 has been cancelled. No new material has been added. Based on the amendment to claim 14 and cancellation of claim 31, Applicant respectfully asserts that the claims are sufficiently definite as required under 35 U.S.C. 112.

Claims 14, 19, 20 and 21 are objected to as they contain terms lacking sufficient antecedent basis. Based upon the amendments to these claims. Applicants respectfully submit that all elements of these claims have appropriate antecedent basis.

II. Claim rejections under 35 U.S.C. § 102

Independent claims 1, 12 and 29 and their dependent claims stand rejected under 35 U.S.C. § 102(a) as being anticipated by "Checking Safety Properties Using Induction and a SAT-Solver" by M. Sheeran, S. Singh and G. Stålmarck. (hereinafter the "Sheeran" reference).

To briefly state the standard, rejections under Section 102 are proper only when the claimed subject matter is identically disclosed or described in the prior art. That is, one unit of prior art must contain all of the material elements recited in the rejected claim. In re Marshall, 198 USPQ 344 (CCPA 1978).

Claim 1 has been amended to recite at least the following elements:

> (a) performing bounded verification on a circuit design for a number of transitions;
> (b) performing induction proof of a first property for the number of transitions, wherein the induction proof is performed by a process comprising the acts of:
> (c) if the at least one property is not verified, then increasing a limit for the bounded verification and repeating from (a).

It is respectfully submitted that the cited Sheeran reference fails to teach, disclose, or suggest this combination of claims elements.

Sheeran is directed to the problem of checking safety properties of large finite state machines using a SAT-solver. The Sheeran reference does not anticipate, teach or suggest that if induction proof of a property fails, then a limit for the bounded verification should be increased and the bounded verification and induction proof repeated as presently recited in claim 1. In fact, the Sheeran reference fails to make any mention, suggestion, or teaching of any increase in a limit of the bounded verification for any reason, much less an increase based failure to verify a property as recited in claim 1.

The Office Action at page 9 cites page 112 of Sheeran and asserts that this section of Sheeran teaches that if the bounded verification and the induction proof are insufficient to determine the one or more properties of the circuit design to be verified, increasing the first number of transitions by increasing "i" (iterations) and finding the condition where state satisfy the property.

In Sheeran, the "i" variable is merely a variable that corresponds to a set of states $s_{[0..i]}$ that is checked using a SAT-solver to determine if the system is P-safe. The variable "i" is incremented to transition through the set of states. There is no teaching that "i" is a limit of a bounded verification, much less that such a limit can be increased if there is a failure to verify a property.

In fact, the Sheeran reference quite clearly teaches away from the concept of even having a limit on the safety property determination. This reference teaches that the iteration of "i" will continue to be incremented, without limit, until the system has been found to be P-safe. As such, Sheeran teaches using an exhaustive number of transitions to reach all states.

For at least these reasons, it is respect fully submitted that claim 1 and its dependent claims are allowable over the cited references. For at least the same reasons, it is respectfully submitted that independent claims 12 and 29, and their dependent claims, are similarly allowable over the cited references.

In addition, amended claim 29 and its dependent claims teach "attempting bounded verification of one or more properties of a circuit design for at least a first predetermined number of transitions". The Sheeran reference does not anticipate, teach or suggest predetermined

number of transitions. As noted above, Sheeran teaches using an exhaustive number of transitions to reach all states.

CONCLUSION

Based on the foregoing, all claims are believed allowable, and an allowance of the claims is respectfully requested. If the Examiner has any questions or comments, the Examiner is respectfully requested to contact the undersigned at the number listed below.

If the Commissioner determines that additional fees are due or that an excess fee has been paid, the Patent Office is authorized to debit or credit (respectively) Deposit Account No. **50-2518**, billing reference no. **7038392001**.

Respectfully submitted,
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